TPS566231, TPS566238 3-V to 17-V Input, 6-A Synchronous Step-Down Voltage Regulator

1 Features

- Auto-skip mode (TPS566231) and continuous current mode (TPS566238)
- Input voltage range: 3 V to 17 V
- Output voltage range: 0.6 V to 7 V
- D-CAP3™ architecture control for fast transient response
- 0.6-V ±1% reference voltage (25°C)
- Supports 6-A continuous output current
- Integrated 20.8-mΩ and 10.6-mΩ $R_{DS(on)}$ internal power switch
- ULQ™(Ultra Low Quiescent current) feature in TPS566231 to enable long battery life
- Eco-Mode™ for light-load running to achieve high efficiency in TPS566231
- 600-kHz switching frequency
- Supports up to 98% duty operation
- Adjustable soft-start time by SS pin
- Built-in output discharge function
- Cycle-by-cycle over current protection
- Non-latched for OC, OV, UV and OT protections
- Small 1.5-mm × 2.0-mm HotRod™ QFN package

2 Applications

- Digital TV, set-top box, gaming consoles
- Server, storage and networking point-of-load
- Industrial PC and factory automation applications
- Distributed power systems with typical 3.3-V, 5-V, 12-V, 15-V input

3 Description

The TPS566231 and TPS566238 are simple, easy to use, high-efficiency, 6-A synchronous buck converters in QFN 9-pin 1.5-mm x 2.0-mm package.

The devices operate with wider supply input voltage ranging from 3 V to 17 V. They use DCAP3™ control mode to provide a fast transient response, good line, load regulation, no requirement for external compensation, and support low ESR output capacitors.

TPS566231 operates in Eco-Mode, which maintains high efficiency during light load operation. One of the key features of the TPS566231 is its ULQ (Ultra Low Quiescent) to enable low-bias current. This feature is extremely beneficial for long battery life in low power operation.

TPS566238 operates in continuous current mode, which maintains lower output ripple during all load conditions.

TPS566231 and TPS566238 can support upto 98% duty cycle operation. They provide complete protection OVP, OCP, UVLO, OTP and UVP with auto-retry.

The TPS566231 and TPS566238 are available in a 9-pin 1.5-mm x 2.0-mm HotRod™ package and the junction temperature is specified from -40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS566231	VQFN (9)	1.50 mm × 2.00 mm
TPS566238		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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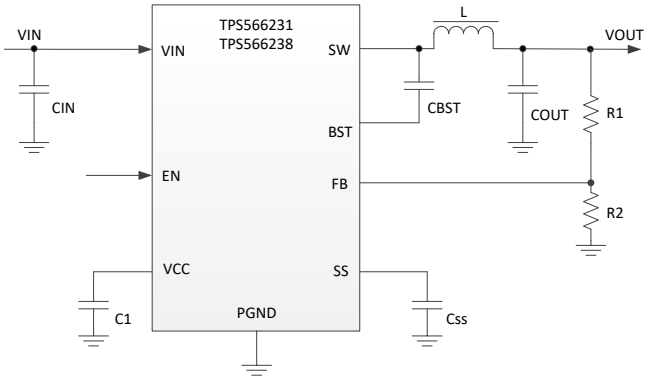
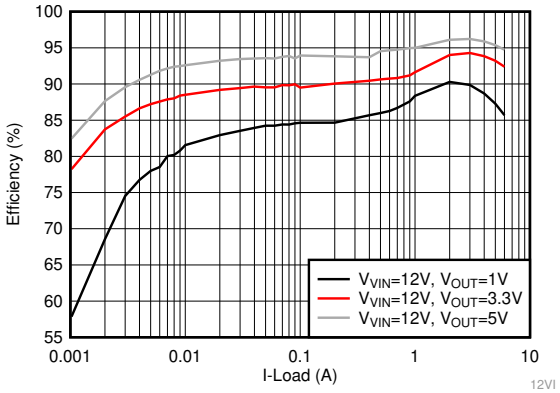
Typical Application



TPS566231 Efficiency vs Output Current



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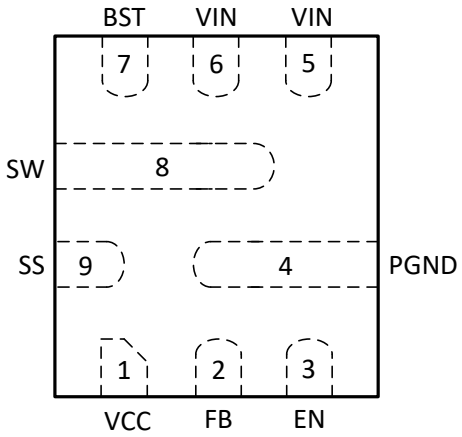
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2020	*	Advance Information release.

5 Pin Configuration and Functions

RQF Package
9-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VCC	1	O	5.0-V internal VCC LDO output. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 1-μF capacitor. If V_{VIN} is lower than 5V, the VCC will follow the VIN voltage.
FB	2	I	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and ground.
EN	3	I	Enable pin of buck converter. EN pin is a digital input pin, decides turn on or off buck converter. Internal pull up current to enable converter if leave this pin open.
PGND	4	G	Power Ground terminal for the controller circuit and the internal circuitry.
VIN	5,6	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
BST	7	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BST and SW, 0.1uF is recommended.
SW	8	O	Switch node terminal. Connect the output inductor to this pin.
SS	9	O	Soft-start time selection pin. Connecting an external capacitor sets the soft-start time.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Input voltage	VIN	–0.3	20	V
		BST	–0.3	26	V
		BST (20-ns transient)	-0.3	28	V
		BST-SW	–0.3	7	V
		SS, FB, EN	–0.3	6	V
		PGND	–0.3	0.3	V
	Output voltage	SW	–2	20	V
		SW (20-ns transient)	–3	22	V
		VCC	–0.3	6	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage	VIN	3	17	V
		BST	–0.1	22.5	V
		BST-SW	–0.1	5.5	V
		SS,FB, EN	–0.1	5.5	V
		PGND	–0.1	0.1	V
	Output voltage	SW	–1	17	V
		SW (20-ns transient)	–2	19	V
		VCC	–0.1	5.5	V
I_{OUT}	Output current		0	6	A
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS566231,TPS566238 RQF(VQFN) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.6	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance with TI EVM	44	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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Thermal Information (continued)

THERMAL METRIC(1)		TPS566231,TPS566238 RQF(VQFN) 9 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	25	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	24.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

6.5 Electrical Characteristics

T_J = -40°C to 125°C, V_{VIN}=12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range	VIN	3		17	V
I_{VIN}	VIN Supply Current	No load, V_{EN}=5V, non-switching (TPS566231)	25	50	75	µA
		No load, V_{EN}=5V, non-switching (TPS566238)	295	395	495	µA
I_{INSDN}	VIN Shutdown Current	No load, V_{EN}=0V		3.2	6	µA
UVLO						
UVLO	VIN Undervoltage Lockout	Wake up VIN voltage	2.7	2.8	2.94	V
UVLO	VIN Undervoltage Lockout	Shut down VIN voltage	2.55	2.6	2.71	V
UVLO	VIN Undervoltage Lockout	Hysteresis VIN voltage		200		mV
VCC OUTPUT						
V_{CC}	VCC Output Voltage	V_{VIN}=12V	4.74	5	5.2	V
V_{CC}	VCC Output Voltage	V_{VIN}= 3V		3		V
I_{CC}	VCC Current Limit	V_{VIN}=12V	20			mA
		V_{VIN}= 3V	5			mA
FEEDBACK VOLTAGE						
VFB	FB voltage	T_J=25°C	596	600	604	mV
VFB	FB voltage	T_J=-40°C to 125°C	591	600	611	mV
MOSFET						
$R_{DS(ON)HI}$	High-side MOSFET Rds(on)	T_J=25°C, V_{VIN}≥5V		20.8		mΩ
		T_J=25°C, V_{VIN}=3V		25.8		mΩ
$R_{DS(ON)LO}$	Low-side MOSFET Rds(on)	T_J=25°C,V_{VIN}≥5V		10.6		mΩ
		T_J=25°C, V_{VIN}=3V		13		mΩ
I_{OCL}	Over Current threshold	Valley current set point	6	7.4	9	A
I_{NOCL}	Negative Over Current threshold			3.4		A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching Frequency	T_J=25°C, V_{VOUT} =1.0V		600		kHz
$T_{ON(MIN)}$	Minimum On-time	T_J=25°C		50		ns
$T_{OFF(MIN)}$	Minimum Off-time(1)	V_{FB}=0.5V		100		ns
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN Threshold High-level		1.17	1.23	1.29	V
$V_{EN(OFF)}$	EN Threshold Low-level		1.05	1.13	1.19	V
V_{ENHYS}	EN Hystersis			100		mV
I_{EN}	EN Pull up Current	V_{EN} = 1.0V		2		uA
OUTPUT DISCHARGE and SOFT START						
R_{DIS}	Discharge resistance	T_J=25°C, V_{VOUT} =0.5V, V_{EN}=0V		114		Ω

(1) No production test, guaranteed by design.

ADVANCE INFORMATION

Electrical Characteristics (continued)

T_J = -40°C to 125°C, V_{VIN}=12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SS}	Soft-start Charge Current			5		uA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP Trip Threshold		110	115	122	%
t_{OVPDLY}	OVP Prop deglitch	T_J=25°C		32		us
V_{UVP}	UVP Trip Threshold		55	60	65	%
t_{UVPDLY}	UVP Prop deglitch			256		us
t_{UVPDEL}	Output Hiccup delay relative to SS time	UVP detect		256		us
t_{UVPEN}	Output Hiccup enable delay relative to SS time	UVP detect		7		cycles
THERMAL PROTECTION						
T_{OTP}	OTP Trip Threshold(1)			160		°C
T_{OTPHSY}	OTP Hysteresis(1)			20		°C

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6.6 Typical Characteristics

T_J=-40°C to 125°C, V_{VIN}=12V(unless otherwise noted)

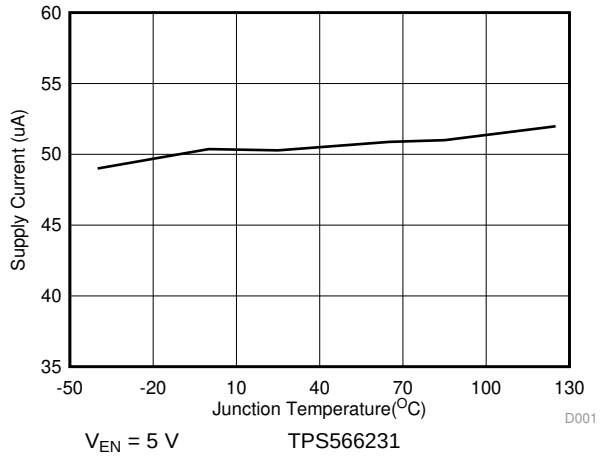


Figure 1. Supply Current vs Junction Temperature

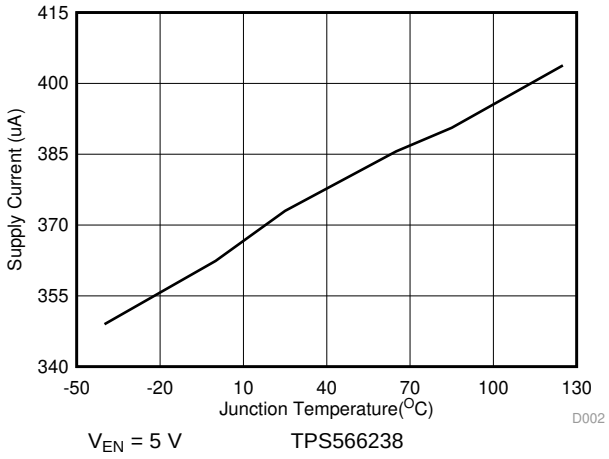


Figure 2. Supply Current vs Junction Temperature

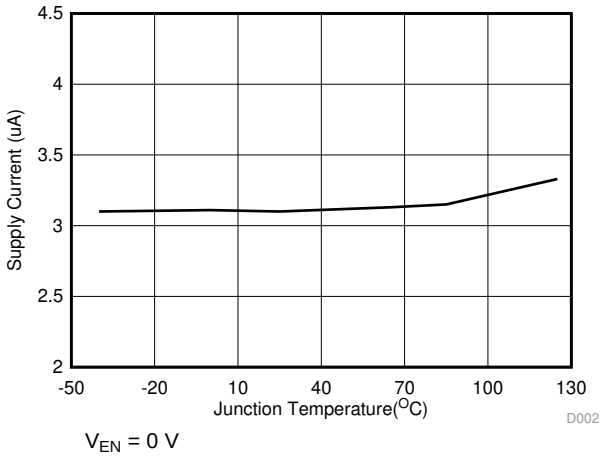


Figure 3. Shutdown Current vs Temperature

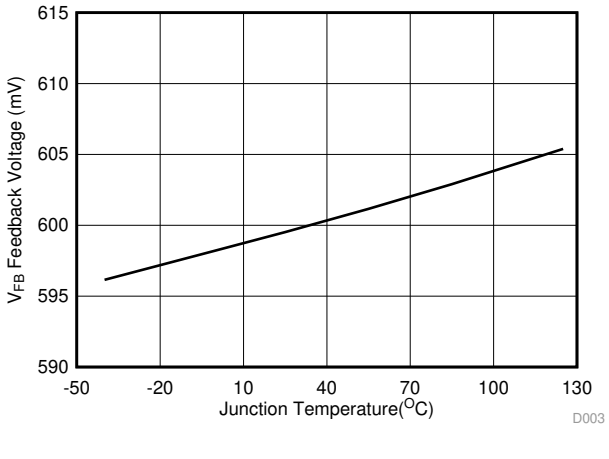


Figure 4. Feedback Voltage vs Junction Temperature

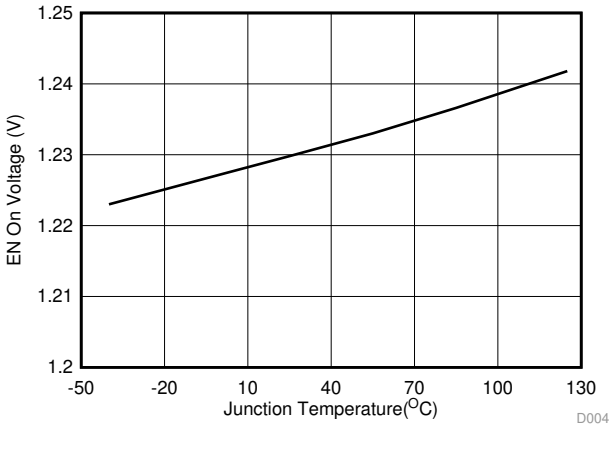


Figure 5. Enable On Voltage vs Junction Temperature

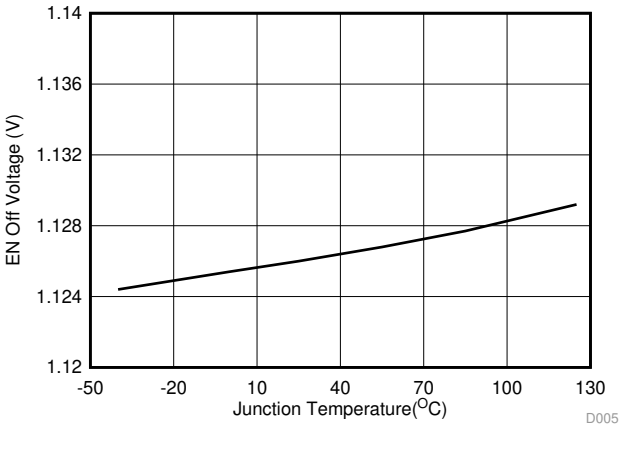


Figure 6. Enable Off Voltage vs Junction Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

T_J=-40°C to 125°C, V_{VIN}=12V(unless otherwise noted)

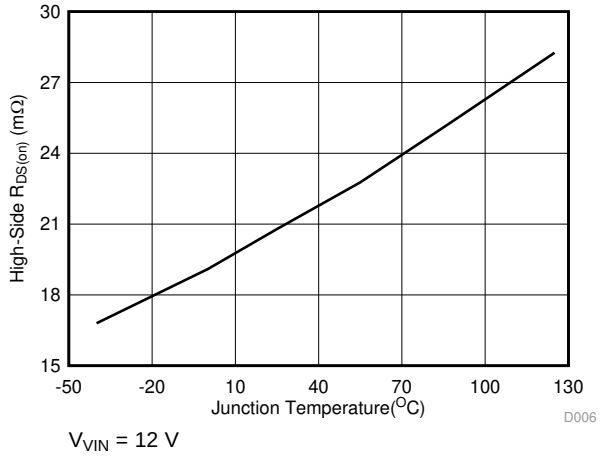


Figure 7. High-Side R_{DS}(on) vs Junction Temperature

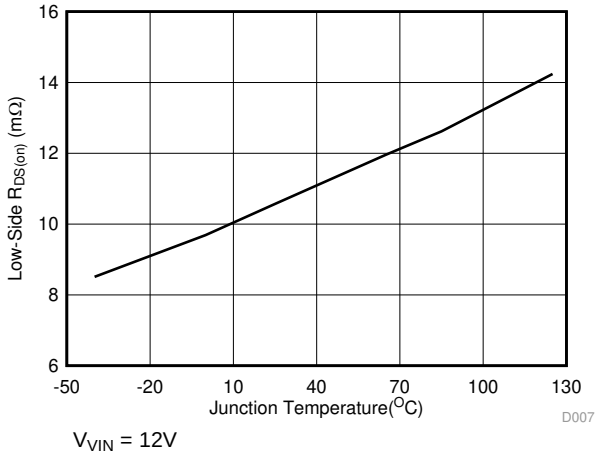


Figure 8. Low-Side $R_{DS(on)}$ vs Junction Temperature

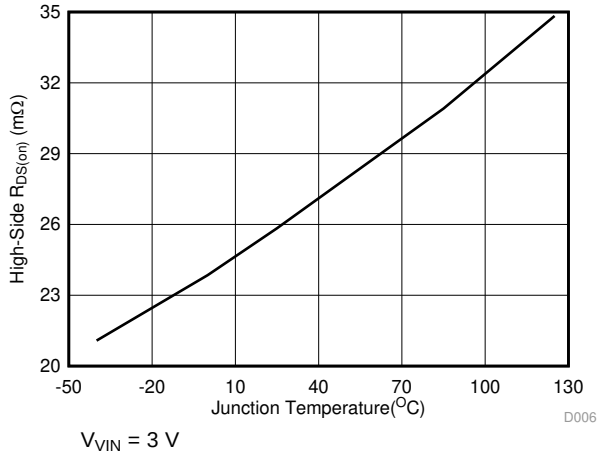


Figure 9. High-Side R_{DS}(on) vs Junction Temperature

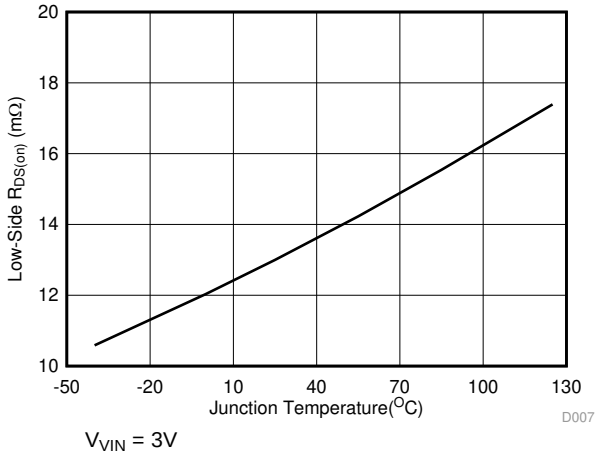


Figure 10. Low-Side $R_{DS(on)}$ vs Junction Temperature

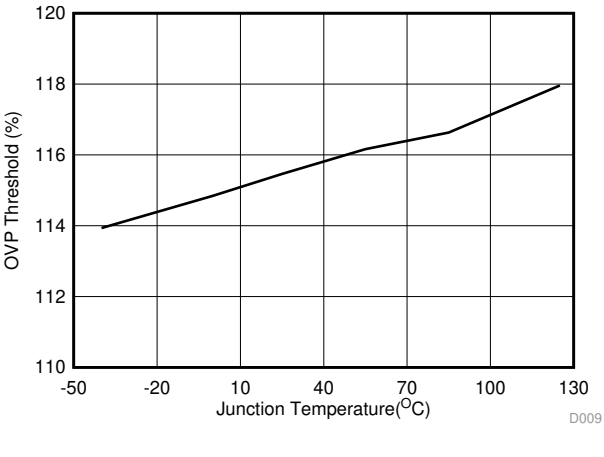


Figure 11. OVP Threshold vs Junction Temperature

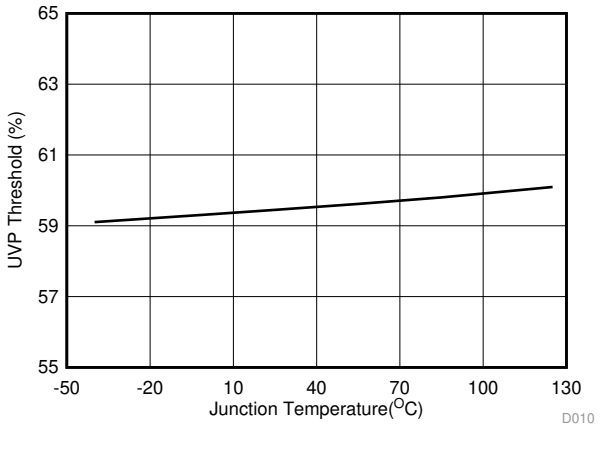


Figure 12. UVP Threshold vs Junction Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

T_J=-40°C to 125°C, V_{VIN}=12V(unless otherwise noted)

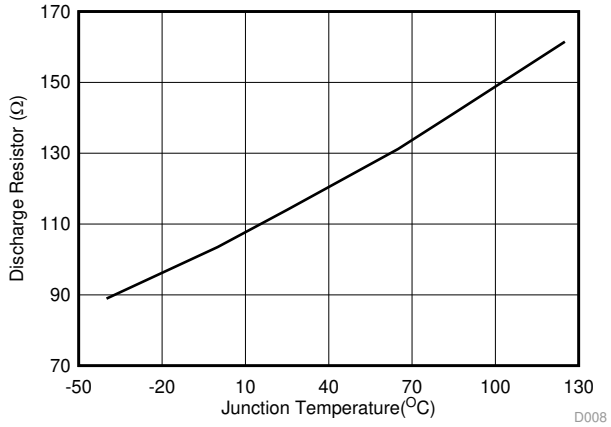


Figure 13. Discharge Resistor vs Junction Temperature

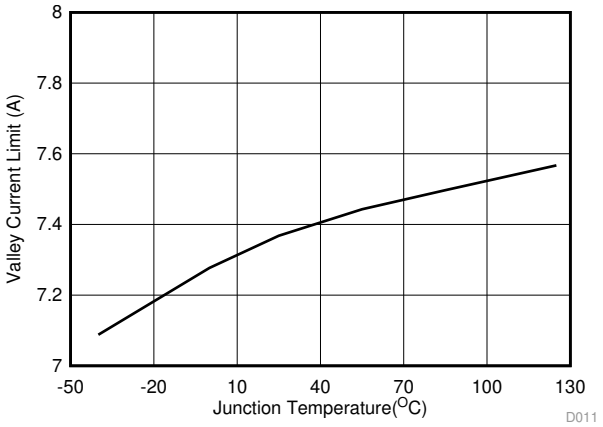


Figure 14. Valley Current Limit vs Junction Temperature

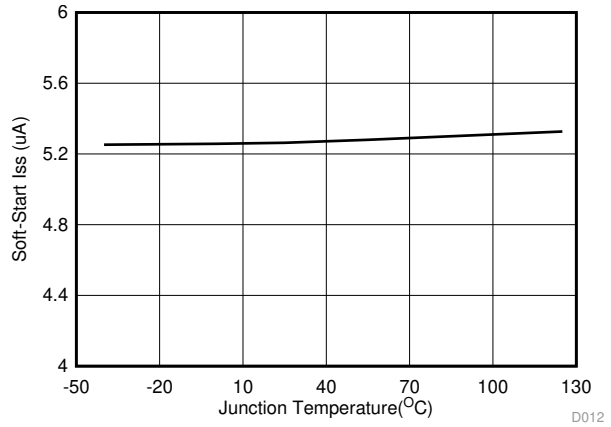


Figure 15. Soft-Start Charge Current Iss vs Junction Temperature

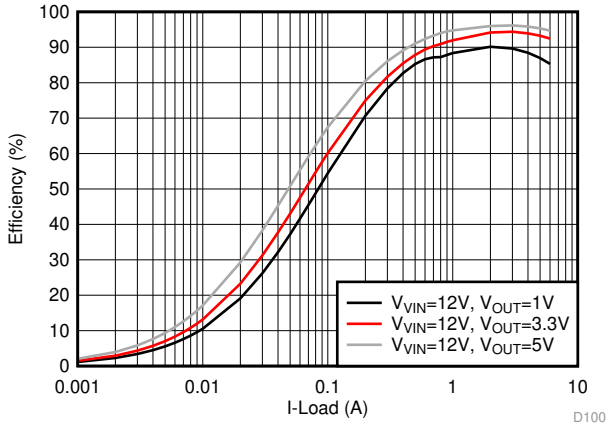


Figure 16. TPS566238 Efficiency

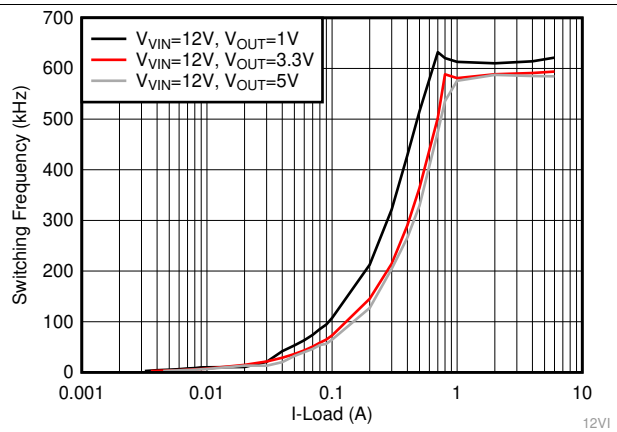


Figure 17. TPS566231 F_{SW} Load Regulation

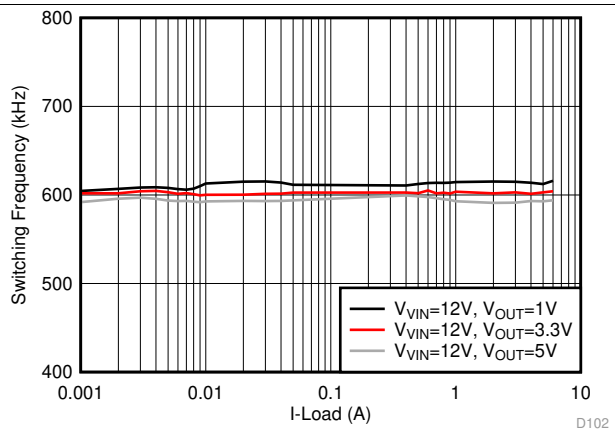


Figure 18. TPS566238 F_{SW} Load Regulation

ADVANCE INFORMATION

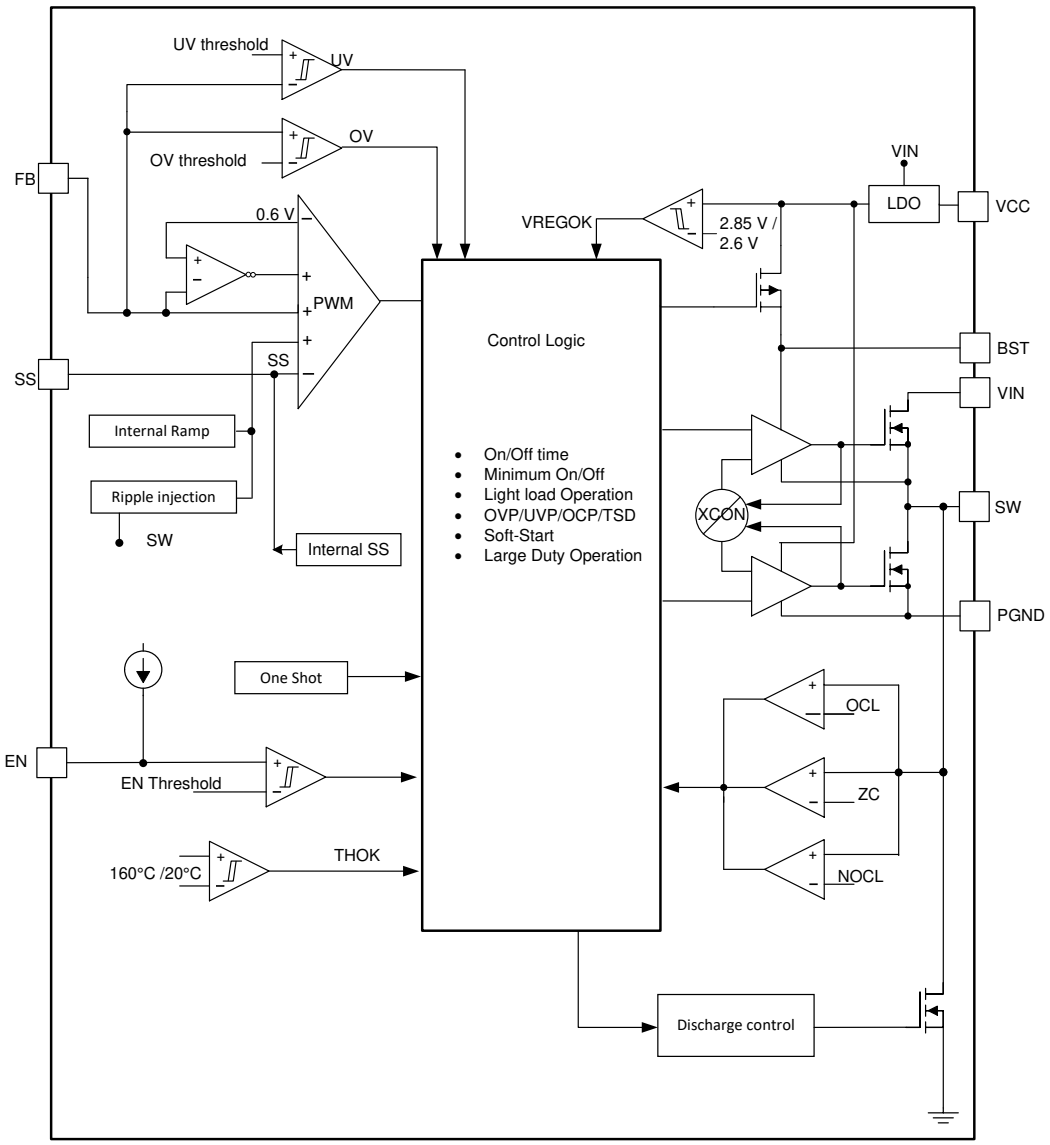
7 Detailed Description

7.1 Overview

The TPS566231 and TPS566238 are 6-A integrated FET synchronous buck converters which operate from 3V to 17V input voltage (V_{IN}), and the output is from 0.6V to 7V. The proprietary D-CAP3™ mode enables low external component count, ease of design, optimization of the power design for cost, size and efficiency. The key feature of the TPS566231 is ultra-low quiescent current (ULQ™) mode. This feature is beneficial for long battery life in system standby mode and achieves high efficiency under light load condition. The devices employ D-CAP3™ mode control that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition.

This Eco-mode™ allows the TPS566231 to maintain high efficiency at light load. The TPS566238 works in continuous current mode allows the converter maintains lower output ripple in all load conditions. The devices are able to adapt to both low equivalent series resistance (ESR) output capacitors such as POS-CAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the buck is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3™ mode control. The DCAP3™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS566231 and TPS566238 also include an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3™ control topology.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the devices is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in Equation 1.

$$f_p = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS566231 and TPS566238. The low-frequency L-C double pole has a 180 degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is about 45-kHz. The inductor and capacitor selected for the output filter is recommended such that the double pole is located close to 1/3 the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (F_{SW}).

7.3.2 Soft Start

The TPS566231 and TPS566238 have an external SS pin is provided for setting higher soft-start time. When the EN pin becomes high, the soft-start function begins ramping up the reference voltage to the PWM comparator.

If the application needs a larger soft start time than 0.5ms, it can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and Ground. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The estimated equation for the soft-start time (T_{SS}) is shown in Equation 2:

$$T_{ss}(ms) = \frac{1.4 \times C_{ss}\ (nF) \times V_{REF}\ (V)}{I_{ss}(uA)} \quad (2)$$

where

- V_{REF} is 0.6 V and I_{SS} is 5 µA

7.3.3 Large Duty Operation

The TPS566231 and TPS566238 can support large duty operations by smoothly dropping down the switching frequency. When the V_{IN}/V_{OUT} <1.6, and the V_{FB} is lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make T_{ON} to be extended to implement the large duty operation and also improve the performance of the load transient performance. The minimum switching frequency is limited with about 165kHz,with typical minimum off time 100ns, the TPS566231 and TPS566238 can support up to 98% duty cycle operation.

ADVANCE INFORMATION

Feature Description (continued)

7.3.4 Over Current Protection and Undervoltage Protection

The TPS566231 and TPS566238 have the over current protection and undervoltage protection. The output over current limit (OCL) is implemented using a cycle-by-cycle valley detect circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over current protection. When the load current is higher than the over current threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the device will shut off after a wait time of 256us and then re-start after the hiccup time (typically 7*Tss). When the over current condition is removed, the output will be recovered.

7.3.5 Over Voltage Protection

The TPS566231 and TPS566238 have the over voltage protection feature. When the output voltage becomes higher than 115% of the target voltage, the OVP is triggered, the output will be discharged after a wait time of 32 µs. When the over voltage condition is removed, the output voltage will be recovered.

7.3.6 UVLO Protection

Undervoltage Lockout protection (UVLO) monitors the V_{VIN} power input. When the voltage is lower than UVLO threshold voltage, the device is shut off and output is discharged. This is a non-latch protection.

7.3.7 Output Voltage Discharge

The TPS566231 and TPS566238 have the discharge function by using internal MOSFET about 114Ω $R_{DS(on)}$, which discharges the output V_{OUT} through SW node during any event like output overvoltage protection, output undervoltage protection , TSD , if VCC voltage below the UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold. The discharge is slow due to the lower current capability of the MOSFET.

7.3.8 Thermal Shutdown

The TPS566231 and TPS566238 monitor the internal die temperature. If the temperature exceeds the threshold value (typically 160°C), the device is shut off and the output will be discharged. This is a non-latched protection, the device restarts switching when the temperature goes below the thermal shutdown threshold.

7.4 Device Functional Modes

7.4.1 Advanced Eco-mode™ Control

The TPS566231 operates in advanced Eco-mode™ mode, the advanced Eco-mode™ control scheme to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode™ operation happens ($I_{OUT(LL)}$) can be calculated from Equation 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

ADVANCE INFORMATION

Device Functional Modes (continued)

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit.

7.4.2 Force CCM Mode

The TPS566238 operates in Force CCM(FCCM) mode which keeps the converter to operate in continuous conduction mode during light-load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (FSW) is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

7.4.3 Standby Operation

The TPS566231 and TPS566238 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 2 µA when in standby condition. EN pin is pulled high internally, when float, the part is enabled by default.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The schematic of Figure 19 shows a typical application for TPS566231 with 1-V output. This design converts an input voltage range of 3 V to 17 V down to 1 V with a maximum output current of 6 A.

8.2 Typical Application

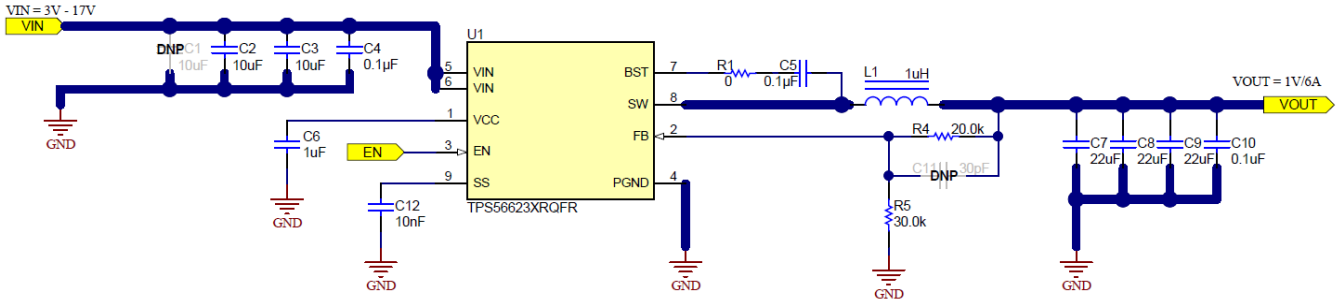


Figure 19. 1-V, 6-A Reference Design

8.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Output voltage			1		V
I_{OUT}	Output current			6		A
ΔV_{OUT}	Transient response	0.1 A - 6 A load step,2.5A/us		±50		mV
V_{IN}	Input voltage		3	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple	CCM condition		14		$mV_{(P-P)}$
F_{SW}	Switching frequency			600		kHz
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor the user can change the output voltage above 0.6 V. See Equation 4

$$V_{OUT} = 0.6 \times (1 + \frac{R_{UPPER}}{R_{LOWER}}) \quad (4)$$

8.2.2.1.2 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See Table 2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 5 and Equation 6. It is important that the inductor is rated to handle these currents.

$$I_{L(RMS)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (5)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{L(ripple)}}{2} \quad (6)$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.3 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In DCAP3™, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 2. It is not recommended to choose the combination of MIN inductance and MIN capacitance or MAX inductance and MAX capacitance.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

Table 2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)			C_{OUT} (µF)		C_{FF} (PF)
			MIN	TYP	MAX	MIN	MAX	
0.6	10	0	0.68	1	4.7	44	220	-
1	30	20	0.68	1	4.7	44	220	-
1.8	20	40	1	1.5	4.7	44	220	0-50
3.3	20	90	1.5	2.2	4.7	44	220	10-100
5.0	30	220	1.5	2.2	4.7	44	220	10-100

ADVANCE INFORMATION

8.2.2.1.4 Input Capacitor Selection

The devices require input decoupling capacitors on power supply input VIN, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in Equation 7.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (7)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of 30 µF on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 8:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (8)$$

A 1-µF ceramic capacitor is needed for the decoupling capacitor on VCC pin.

8.2.3 Application Curves

Figure 20 through Figure 43 apply to the circuit of Figure 19. V_{IN} = 12 V. T_A = 25°C unless otherwise specified.

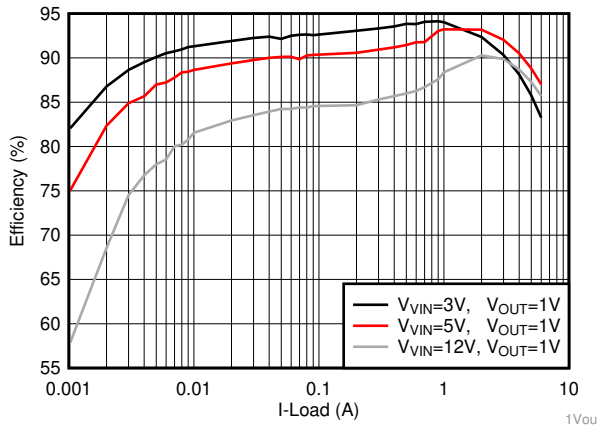


Figure 20. TPS566231 Efficiency Curve

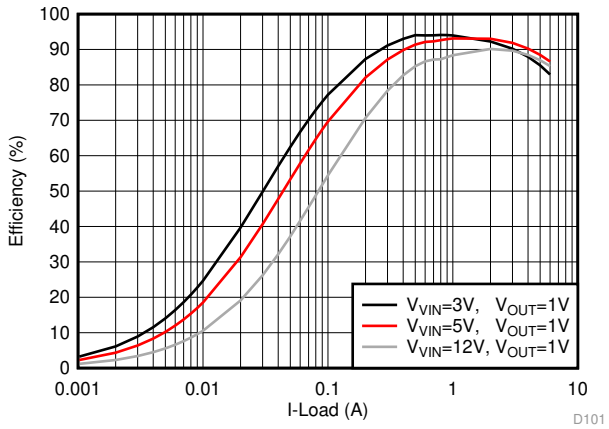


Figure 21. TPS566238 Efficiency Curve

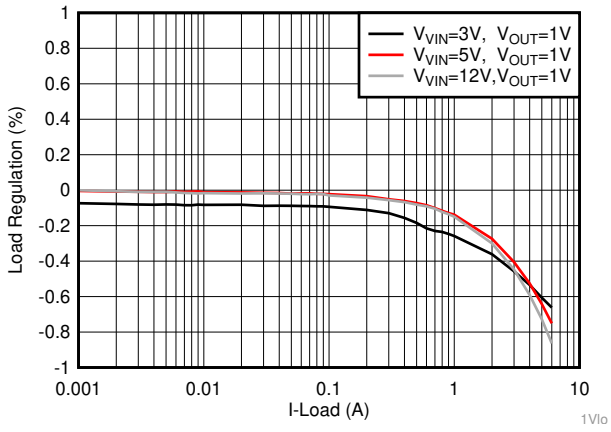


Figure 22. TPS566231 Load Regulation

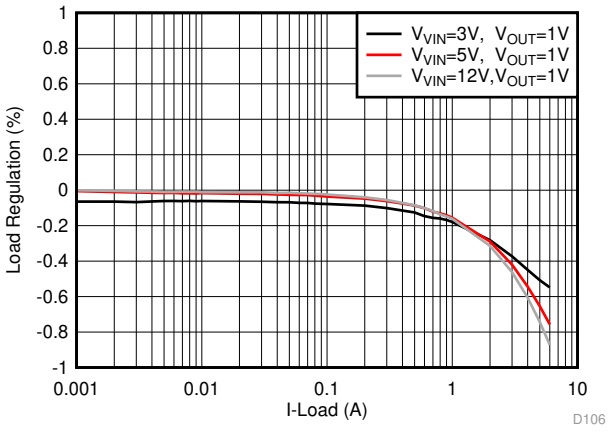


Figure 23. TPS566238 Load Regulation

ADVANCE INFORMATION

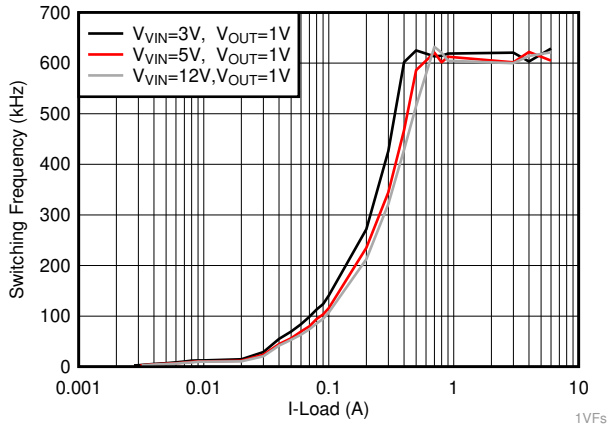


Figure 24. TPS566231 F_{SW} vs Output Load

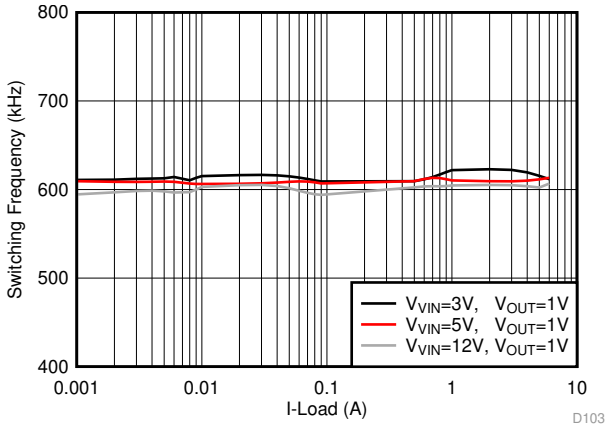
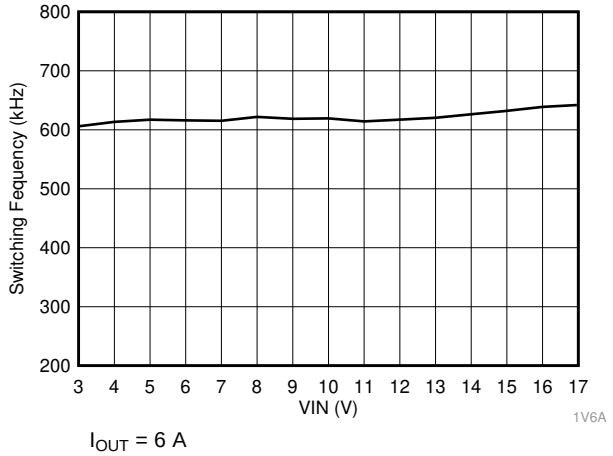


Figure 25. TPS566238 F_{SW} vs Output Load



I_{OUT} = 6 A

Figure 26. Switching Frequency vs Input Voltage

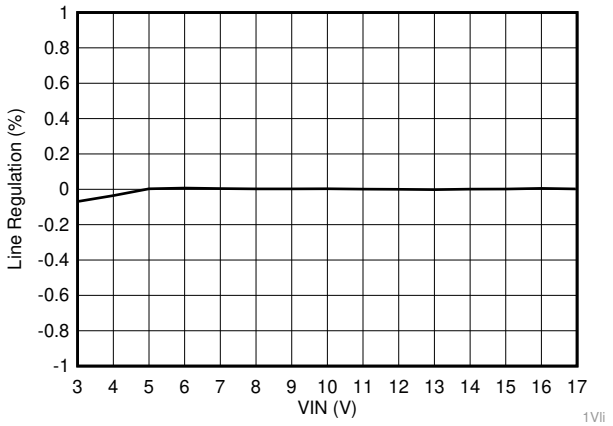


Figure 27. TPS566231 Line Regulation,I_{OUT} = 0.1 A

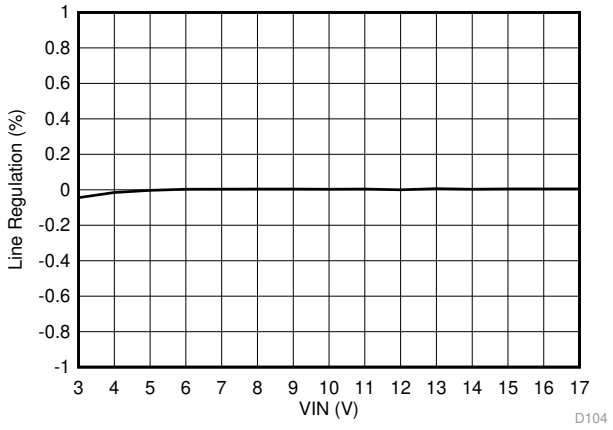


Figure 28. TPS566238 Line Regulation,I_{OUT} = 0.1 A

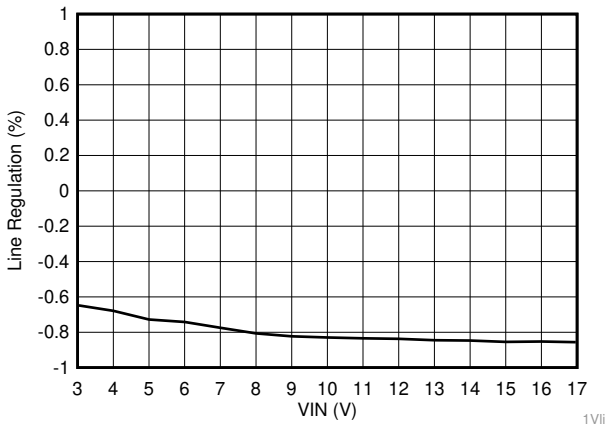


Figure 29. Line Regulation,I_{OUT} = 6 A

ADVANCE INFORMATION

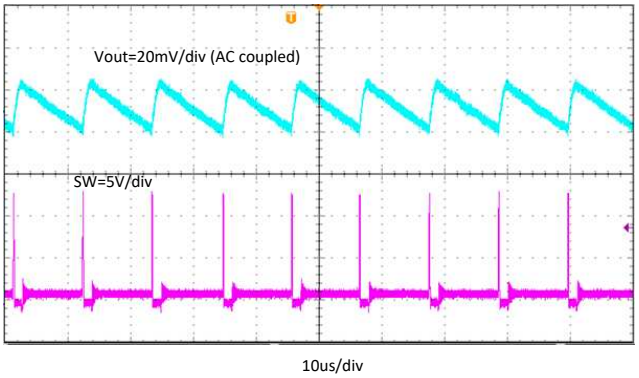


Figure 30. TPS566231 Output Voltage Ripple, I_{OUT} = 0.01 A

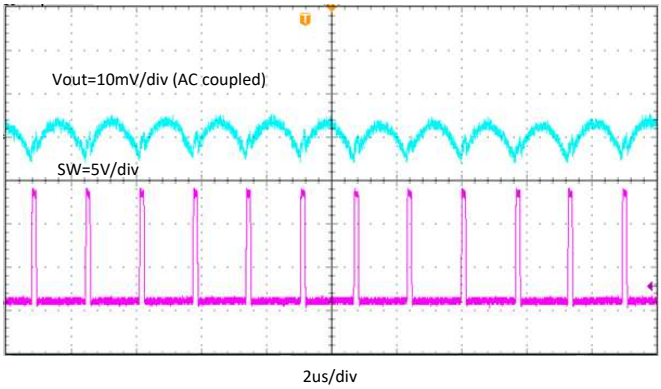


Figure 31. TPS566238 Output Voltage Ripple, I_{OUT} = 0.01 A

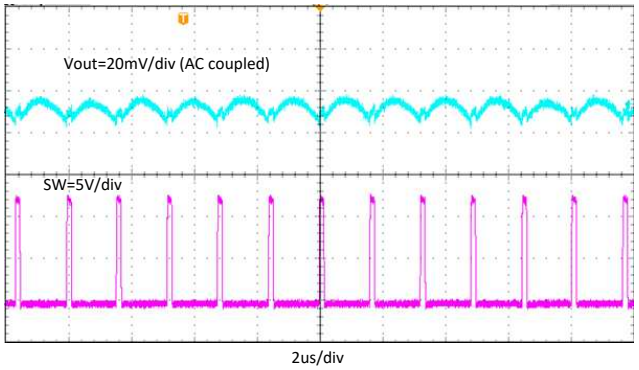


Figure 32. Output Voltage Ripple, I_{OUT} = 6 A

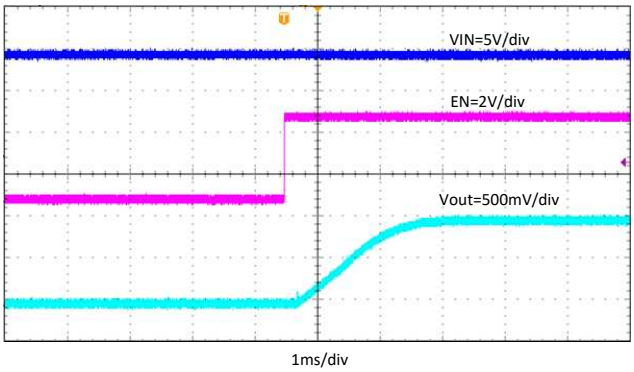


Figure 33. Start-Up Through EN, I_{OUT} = 3A

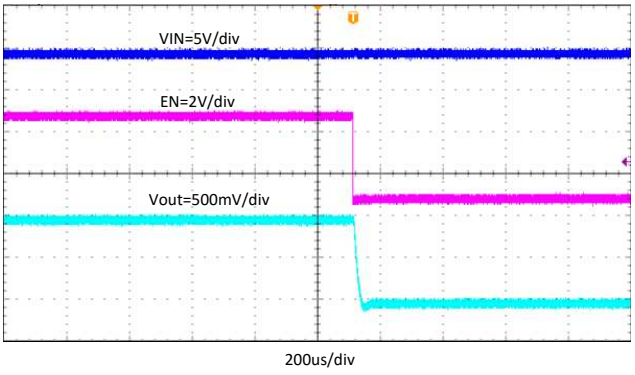


Figure 34. Shut-down Through EN, I_{OUT} = 3A

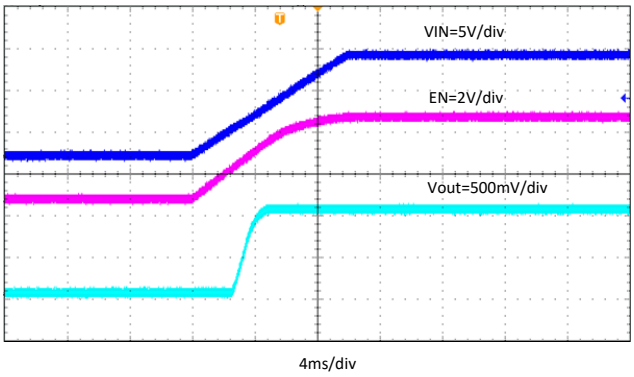


Figure 35. Start Up Relative to V_{IN} Rising, I_{OUT} = 3 A

ADVANCE INFORMATION

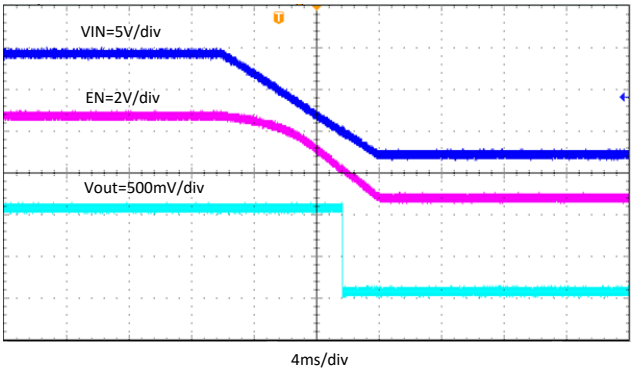
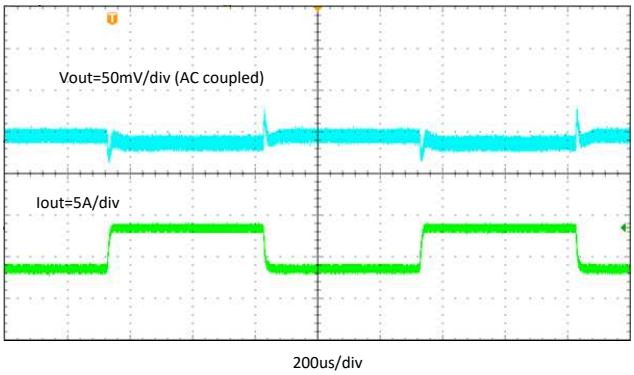
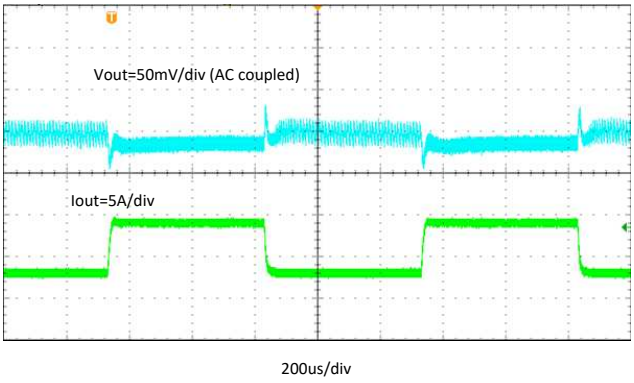


Figure 36. Start Up Relative to V_{IN} Falling, I_{OUT} = 3 A



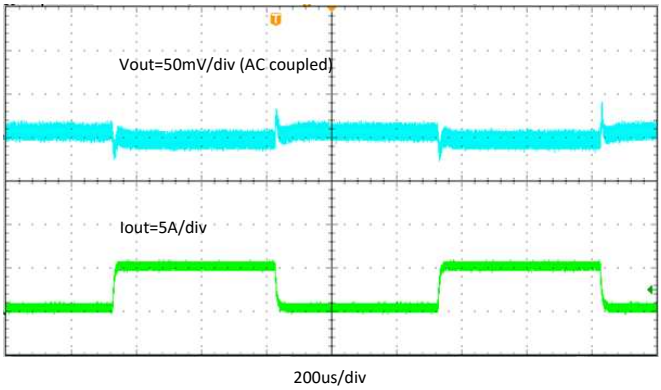
Slew Rate=2.5A/us

Figure 37. TPS566231 Transient Response, 0.6 A to 5.4 A



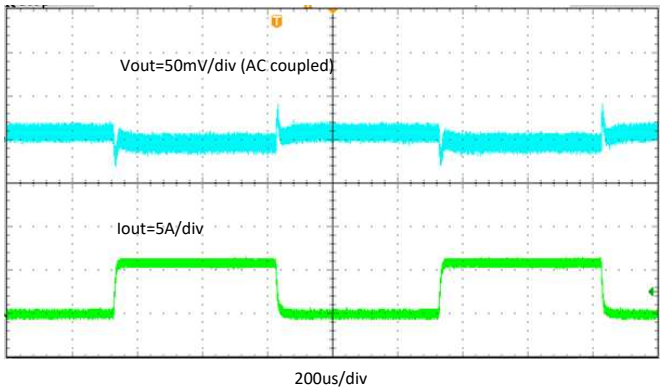
Slew Rate=2.5A/us

Figure 38. TPS566231 Transient Response, 0.1 A to 6 A



Slew Rate=2.5A/us

Figure 39. TPS566238 Transient Response, 0.6 A to 5.4 A



Slew Rate=2.5A/us

Figure 40. TPS566238 Transient Response, 0.1 A to 6 A

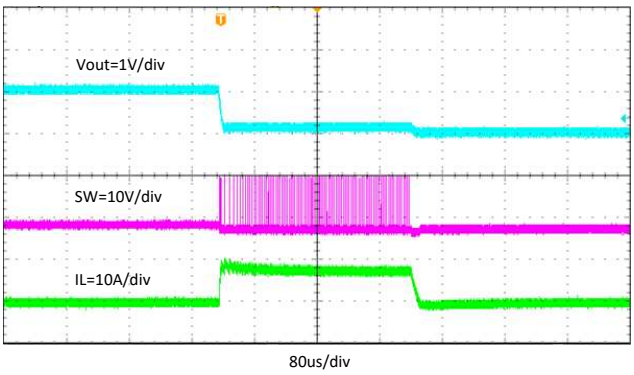


Figure 41. TPS566231 Normal Operation to Output Hard Short

ADVANCE INFORMATION

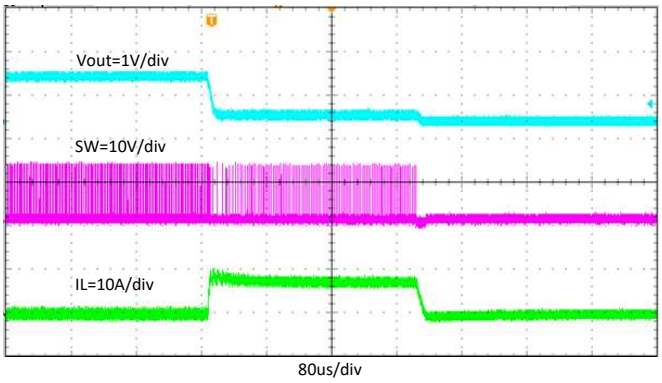


Figure 42. TPS566238 Normal Operation to Output Hard Short

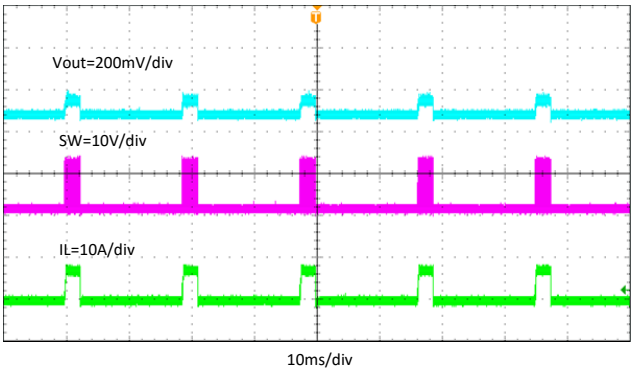


Figure 43. Output Hard Short Hiccup

9 Power Supply Recommendations

The TPS566231 and TPS566238 are intended to be powered by a well regulated dc voltage. The input voltage range is 3 to 17 V. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS566231 and TPS566238 circuit, additional input bulk capacitance is recommended, typical values are 100 μF to 470 μF.

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 55-mm × 60-mm, four-layer PCB with 2-1-1-2 oz copper is used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place output inductor and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the PGND connection of output capacitor and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- Feedback could be 20mil and must be routed away from the switching node, BST node or other high efficiency signal.
- VIN trace must be wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance

10.2 Layout Example

Figure 44 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in Figure 19. Resistor divider for EN is not used in the circuit of Figure 19, but are shown in the layout for reference.

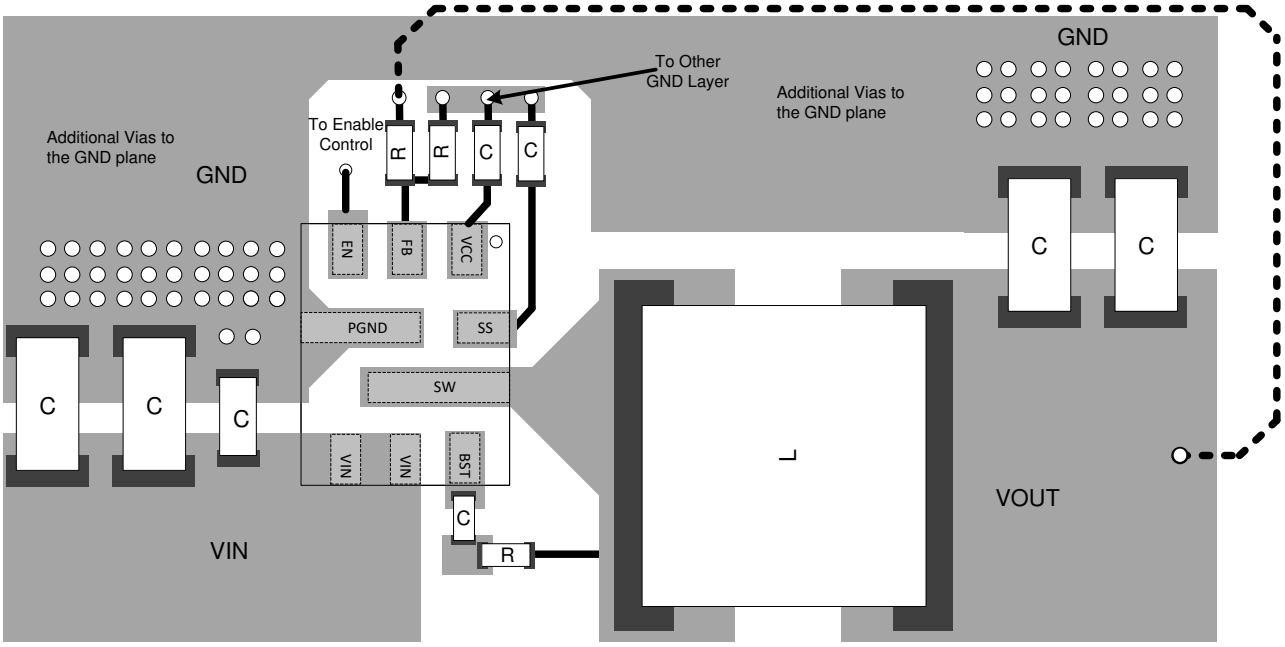


Figure 44. Top-Layer Layout

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11.7 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS566231	Click here	Click here	Click here	Click here	Click here
TPS566238	Click here	Click here	Click here	Click here	Click here

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
XTPS566231RQFR	ACTIVE	VQFN	RQF	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 Year	–40 to 125	X31
XTPS566238RQFR	ACTIVE	VQFN	RQF	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 Year	–40 to 125	X38

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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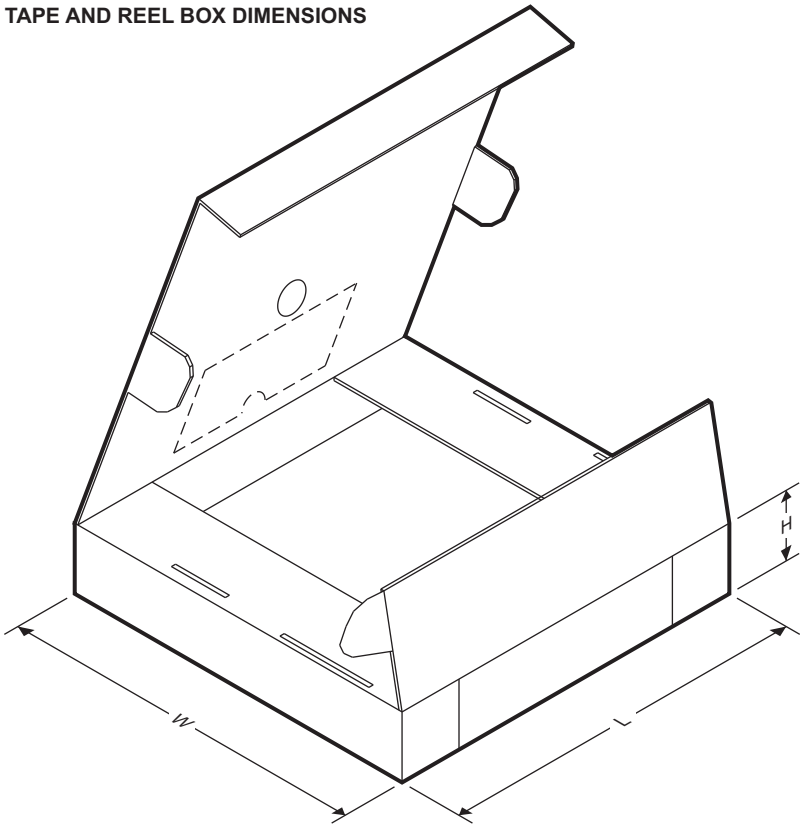
ADVANCE INFORMATION

12.1.2 Tape and Reel Information

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTPS566231RQFR	VQFN	RQF	9	3000	180	8.4	1.75	2.25	1.13	4	5.3	2
XTPS566238RQFR	VQFN	RQF	9	3000	180	8.4	1.75	2.25	1.13	4	5.3	2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTPS566231RQFR	VQFN	RQF	9	3000	210	185	35
XTPS566238RQFR	VQFN	RQF	9	3000	210	185	35

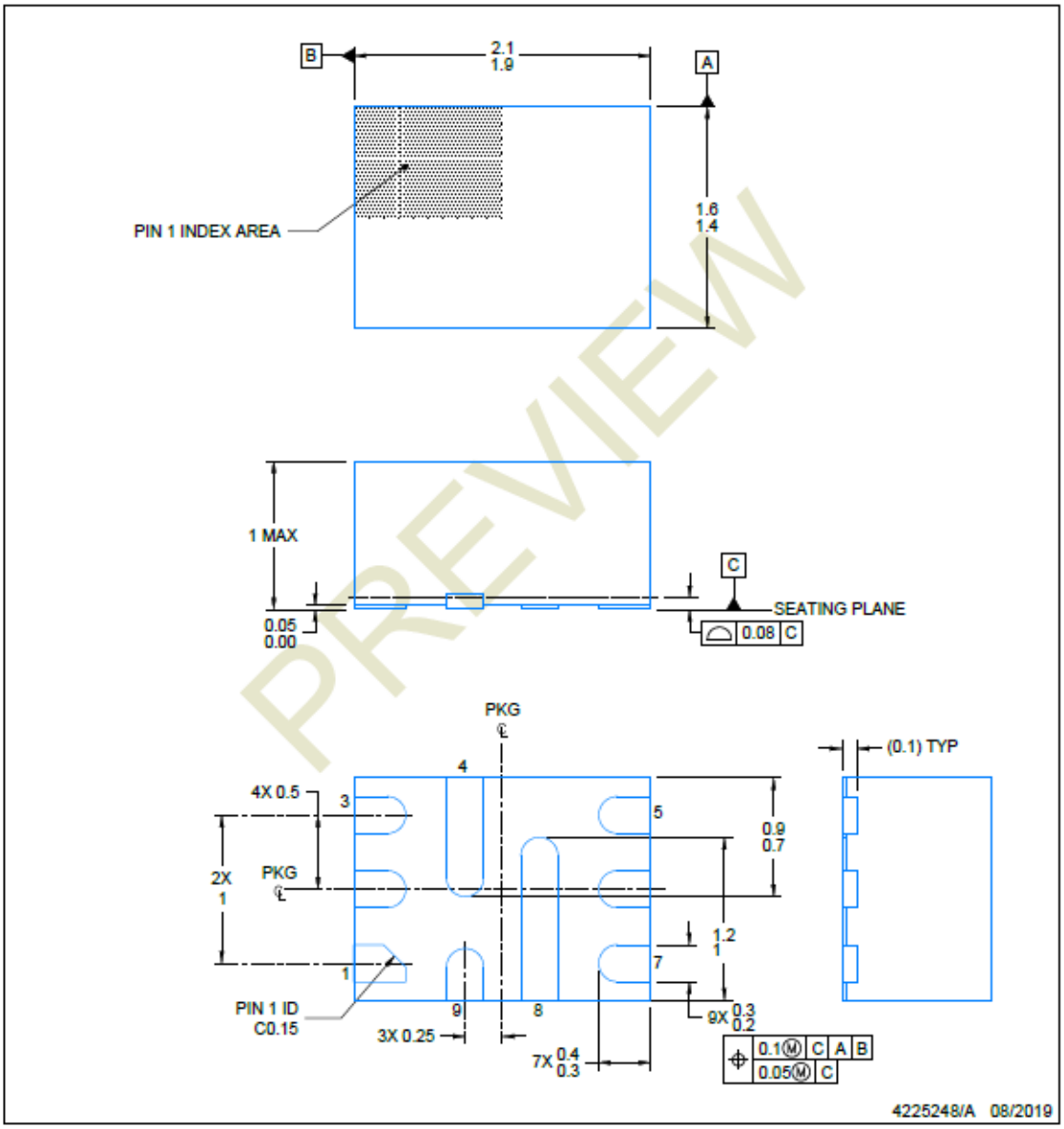
ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

RQF0009A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



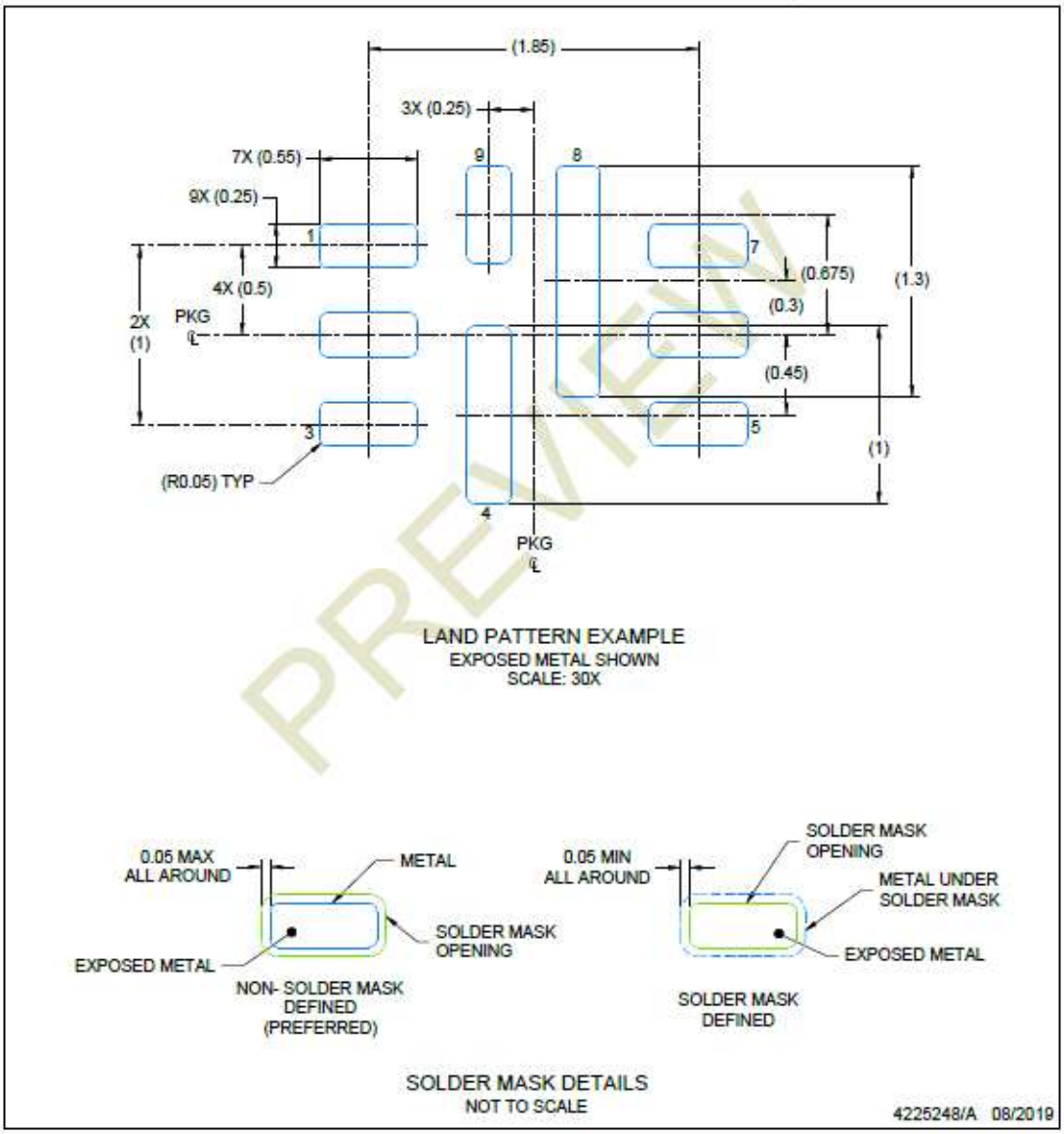
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RQF0009A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



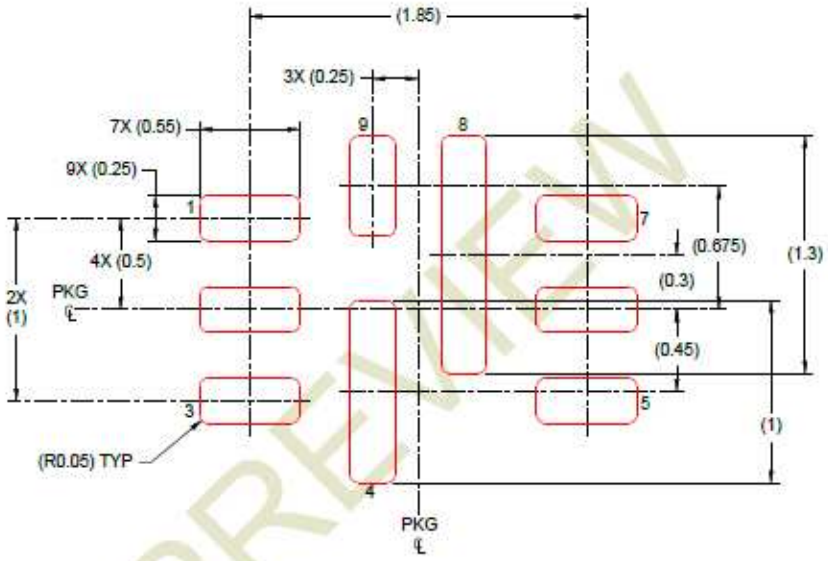
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RQF0009A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 30X

4225248/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS566231RQFR	PREVIEW	VQFN-HR	RQF	9	3000	TBD	Call TI	Call TI	-40 to 125		
TPS566238RQFR	PREVIEW	VQFN-HR	RQF	9	3000	TBD	Call TI	Call TI	-40 to 125		
XTPS566231RQFR	ACTIVE	VQFN-HR	RQF	9	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XTPS566238RQFR	ACTIVE	VQFN-HR	RQF	9	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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